We Claim:

1. An integrated memory, comprising:

a memory cell array for storing data; and

an access controller coupled to and controlling an access to said memory cell array for reading data from, and writing data to, said memory cell array, during a first operating mode said access controller accessing said memory cell array for writing a first data item of an access cycle to said memory cell array with a write latency, during a second operating mode said access controller accessing said memory cell array for writing the first data item of the access cycle to said memory cell array in an accelerated manner without the write latency of the first operating mode, said access controller accessing said memory cell array in accordance with a double data rate specification in the first operating mode and in accordance with a single data rate specification in the second operating mode.

2. The integrated memory according to claim 1, wherein said access controller accesses said memory cell array in the second operating mode for writing the first data item to said memory cell array synchronously with an application of a write command.

3. The integrated memory according to claim 1, further comprising:

an external terminal for receiving data signals;

a data path having at least two data lines coupled to said memory cell array;

a first multiplexer connected between said external terminal and said data path, said data lines of said data path are alternatively connected to said external terminal through said first multiplexer in the first operating mode; and

a second multiplexer disposed in said data path and connected between said first multiplexer and said memory cell array, said data lines being connected, through said second multiplexer, to said first multiplexer in the first operating mode and to said external terminal in parallel in the second operating mode.

4. The integrated memory according to claim 3, further comprising:

a register, which can be written to externally; and a third multiplexer connected to said register and to said external terminal, said data lines may be connected to said register in parallel or to said external terminal in parallel through said second and third multiplexers in the second operating mode.

5. The integrated memory according to claim 3, further comprising:

a multibit register being written to externally; and

a third multiplexer connected to said multibit register and to said external terminal, said data lines may be connected to a respective terminal of said multibit register or to said external terminal in parallel through said second and third multiplexers in the second operating mode.

6. The integrated memory according to claim 1, wherein the first operating mode is a normal mode and the second operating mode is a test mode of the integrated memory.